CLAIMS

What is claimed is:

1   1.   A system, comprising:

2   a voltage regulator and a clock generator to send a processor voltage or a

3   processor clock, respectively;

4   a processor coupled to the voltage regulator to receive the processor voltage

5   and the clock generator to receive the processor clock, respectively;

6   a control signal coupled to the processor, the voltage regulator, and the clock

7   generator to prevent the processor from receiving the processor voltage and the

8   processor clock until a fuse block programmed with a voltage configuration signal and

9   a frequency configuration signal to specify the processor voltage and the processor

10   clock frequency, respectively is determined to have a proper fuse block voltage.

1   2.   The system of claim 1, wherein the voltage regulator is coupled to send the fuse

2   block voltage to the processor and the control signal to the processor and the clock

3   generator.

1   3.   The system of claim 1, further comprising a second voltage regulator coupled

2   to send the fuse block voltage to the processor and the control signal to the first

3   voltage regulator, the processor and the clock generator.

1   4.   The system of claim 1, further comprising a second voltage regulator coupled

2   to send the fuse block voltage to the processor, and wherein the first voltage regulator

3   is coupled to sense the fuse block voltage and to send the control signal to the

4   processor and the clock generator.

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1　5.　　The system of claim 1, further comprising a transistor coupled to invert the

2　control signal and send the inverted control signal to the clock generator.

1　6.　　A system, comprising:

2　　　　a processor having programmable fuse block programmed with at least one

3　configuration signal;

4　　　　logic coupled to the processor to read the configuration signal and in response

5　to generate a value specified by the configuration signal;

6　　　　a control signal coupled to the processor and the logic to prevent the logic from

7　reading the configuration signal until a predetermined event occurs.

1　7.　　The system of claim 6, wherein the configuration signal specifies a voltage for

2　the logic to generate.

1　8.　　The system of claim 6, wherein the configuration signal specifies a frequency

2　for the logic to generate.

1　9.　　The system of claim 6, wherein the predetermined event is when power to the

2　programmable fuse block is valid and stable.

1　10.　　The system of claim 6, wherein the predetermined event is when the

2　configuration signal is valid and stable.

1   11.   A processor, comprising:

2   front-end logic to receive a control signal; and

3   configuration signal logic coupled to the front-end logic to inhibit booting up

4 of the processor in response to the front-end logic receiving the control signal.

1   12.   The processor of claim 11, wherein the configuration signal logic is to inhibit

2 booting up of the processor for a period of time.

1   13.   The processor of claim 11, wherein the configuration signal logic is coupled to

2 the front-end logic to inhibit booting up of the processor for a period of time after the

3 configuration signal logic has power.

1   14.   An apparatus, comprising:

2   a machine-readable medium having stored thereon instructions for causing a

3 processor to:

4   apply a control signal to a processor from a voltage regulator to inhibit a

5 platform normal boot process until at least one configuration signal can be read from a

6 programmable fuse block in the processor.

1   15.   The apparatus of claim 14, wherein the configuration signal specifies a voltage

2 or a frequency to be received by the processor.

1   16.   An apparatus, comprising:

2   a machine-readable medium having stored thereon instructions for causing a

3   processor to:

4   receive a control signal to prevent a computer platform from booting until a

5   voltage applied to a processor fuse block programmed with at least on configuration

6   signal has reached a threshold level;

7   receive the control signal to permit the processor fuse block to be read;

8   configure the processor based on the configuration signals read from the fuse

9   block; and

10   permit the computer platform to boot.

1   17.   The apparatus of claim 16, wherein the instructions are further to cause the

2   processor to receive a core voltage or a system bus clock, respectively, specified by

3   the configuration signals.

1   18.   The apparatus of claim 16, wherein the instructions are further to cause the

2   processor to receive the control signal to permit the processor fuse block to be read

3   when a fuse block voltage has reached a threshold value.

1   19.   The apparatus of claim 16, wherein the instructions are further to cause the

2   processor to receive the control signal to permit a clock generator or a voltage

3   regulator to read the processor fuse block when a fuse block voltage has reached a

4   threshold value.

1   20.   The apparatus of claim 19, wherein the instructions are further to cause the

2   processor to receive a frequency signal or a voltage signal from the clock generator or

3   voltage regulator after the clock generator or voltage regulator reads the processor

4   fuse block.